In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

1. (Original) A field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising

a gate structure formed on said surface of said layer of semiconductor material, and

a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned with said gate structure.

2. (Original) A field effect transistor as recited in claim 1, wherein said discontinuities are self-aligned with said gate structure.

3. (Original) A field effect transistor as recited in claim 1, wherein said discontinuous film is a stressed film

4. (Original) A field effect transistor as recited in claim 3, wherein said stressed film comprises an insulator.

5. (Original) A field effect transistor as recited in claim 1, wherein said discontinuous film comprises an insulator.

6. (Original) A field effect transistor as recited in claim 1, wherein said discontinuous film has a stepped or staircase profile in cross-section.

7. (Original) A field effect transistor as recited in claim 3, wherein said stressed film has a stepped or staircase profile in cross-section.

8. (Original) A field effect transistor as recited in claim 7 wherein said stepped or staircase portion defines an effective channel depth.

9. (Original) A field effect transistor as recited in claim 1, wherein said discontinuous film is an insulator including a portion formed of oxidized SiGe, wherein said discontinuity defines a location of a conductor connected to a channel of said field effect transistor.

10. (Original) A field effect transistor as recited in claim 1, further including a void within said layer of semiconductor material.

11. (Original) An integrated circuit including a field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising

a gate structure formed on said surface of said layer of semiconductor material, and

a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned with said gate structure.

12. (Original) An integrated circuit as recited in claim 11, wherein said discontinuous film has a stepped or staircase profile in cross-section.

13. (Currently Amended) An integrated circuit as recited in claim ~~11~~ 12 wherein said stepped or staircase portion defines an effective channel depth.

14. (Original) An integrated circuit as recited in claim 11, wherein said discontinuous film is an insulator including a portion formed of oxidized SiGe, wherein said discontinuity defines a location of a conductor connected to a channel of said field effect transistor.

15. (Original) An integrated circuit as recited in claim 11, further including a void within said layer of semiconductor material.

16. (Withdrawn) A method of forming a hybrid field effect transistor or integrated circuit comprising steps of

forming a gate structure,

forming a discontinuous layer having a discontinuity aligned with said gate structure within a layer of semiconductor material underlying said gate structure.

17. (Withdrawn) The method as recited in claim 8, wherein said gate structure is formed on a surface of said layer of semiconductor material.

18. (Withdrawn) A method as recited in claim 16, wherein said step of forming a discontinuous layer comprises steps of

developing differential etch rates in respective portions of a continuous layer of semiconductor material,

selectively etching a said portion of said continuous layer to form a void, and

depositing material in said void.

19. (Withdrawn) A method as recited in claim 18, wherein said step of forming said discontinuous layer includes a step of

oxidizing a surface of material exposed within said void.

20. (Withdrawn) A method as recited in claim 18, wherein said step of developing a differential etch rate includes a step of impurity implantation self-aligned with said gate structure.